REMARKS

Claims 1-31 are pending. All stand rejected. By the above amendment, the applicants have amended claims 1, 4, 5, 8-10, 15, 19, 20, 23, 26, 30 and 31 and cancelled claim 25. The applicant requests further examination and consideration in view of the amendments above and remarks set forth below.

The office action states at paragraph 4 that the application was received on August 12, 2001 and that no earlier priority is claimed. The applicants are entitled to priority of the filing date which is August 9, 2001.

Rejections under 35 U.S.C. § 112, Second Paragraph:

Claims 1 and 2 are rejected as being indefinite. The office action at paragraph 14 states that because claim 1 recites "the storage system" and claim 2 recites "a data storage system" it is not clear whether both claims are referring to the same type of storage. In addition, the office action states that the antecedent basis for "the storage system" in claim 1 is not clear. The office action further states that it is not clear how claim 2 further limits claim 1.

In response, the applicants have clarified claims 1 and 2. More particularly, "the storage system" is deleted from claim 1. Thus, claim 1 is directed to a method of assigning resources to for a computer system design. Claim 2 further limits claim 1 by reciting that the computer system design comprises a design for a data storage system. The title has been amended to comport more closely with amended claim 1.

The applicants have also made additional clarifying amendments to claim 1. More particularly, claim 1 is amended to recite that the design includes assignments of system resources to applications and to recite that modifying the design includes modifying the assignments of the system resources. These amendments are supported by the applicants' specification at least at page 2, lines 33-34 and page 8, lines 25-26, where it explains that embodiments of the invention provide a method and apparatus for assignment of resources for a computer system design, and at page 4, line 29 to page 7, line 9, where it explains how the allocations may be made and modified for particular applications.

The applicants have made corresponding amendments to claims 10 and 23.

The office action states in paragraph 15 that in claim 4, the term "utility functions" is not adequately defined. The applicants have amended claim 4 to recite at least one utility function representing utility as a function of one or more of the

performance parameters. This amendment is supported by the applicants' specification at least at page 7, line 5 to page 8, line 11, where the utility functions are explained in detail. The applicants have made corresponding amendments to claims 15 and 26.

The office action states in paragraph 16 that in claims 8 and 9, the terms "first indicia" and "second indicia" are not adequately defined. The applicants have amended claims 8 and 9 to omit these terms. The applicants have made corresponding amendments to claims 1, 19, 20, 30 and 31.

Claim 6 is amended to add a period to its end.

In view of the above, the applicants respectfully submit that the claims are not indefinite.

Rejections under 35 U.S.C. § 112, First Paragraph:

Claims 1-31 are rejected as not being supported by the specification. Particularly, the office action states that "an 'expert system' is defined by Microsoft Computer Dictionary as: 'An application program that makes decisions or solves problems in a particular field, such as finance or medicine, by using knowledge and analytical rules defined by experts in the field. It uses two components, a knowledge base and an inference engine, to form conclusions...'." Having defined an "expert system," the office action further states in paragraph 28 that "all of the claims appear to claim an expert system for circuit design." This is based on the examiner's observation that the recited steps "might" be performed by a person with a Bachelor of Science in Electrical Engineering or similar. The office action alleges that the claims are not enabled because no set of expert rules is provided by which the claimed steps of modifying or predicting would be enabled.

The applicants respectfully traverse the rejection. The premise upon which the rejection is based, i.e. that the claims are directed toward an "expert system," is not correct. This is apparent because the claims do not recite an expert system, a knowledge base, or an inference engine; however, according to the definition of "expert system" quoted in the office action, all of these elements are required for an expert system. Thus, while the office action states that the claims "appear" to be directed toward an expert system, no reasonable basis is provided to support this conclusion. That the claimed steps "might" be performed by a person with a Bachelor of Science degree is not a sufficient basis to support such a conclusion. Rather,

because the claims do not recite an expert system, no teaching of an expert system is required to enable the claims. Therefore, the examiner has not satisfied the initial burden to establish a reasonable basis as to the question of enablement. See Manual of Patent Examining Procedure at Section 2164.05 (8th Ed., Rev. 2). Because the initial burden has not been satisfied, the rejection must be removed.

Further, as explained in detail below, the applicants' specification does contain a teaching of the manner and process of making and using the invention in terms which correspond in scope to those used in the claims without requiring the use of an "expert system." Taking claim 1 as an example, it is directed toward a method of assigning resources for a computer system design. As explained in the applicants' specification at least at page 2, lines 33-34 and page 8, lines 25-26, embodiments of the invention provide a method of and apparatus for assignment of resources for a computer system design.

Claim 1 recites a step of:

receiving desired levels of performance parameters for a computer system design from a user via a user interface to a computer system, the design including assignments of system resources to applications...

The applicants' specification at page 9, lines 12-14, explains that the user may specify desired measures of performance for each application by making selections from a menu shown on the display 100 (Figure 1). To further illustrate this step, the applicants' specification describes in detail an example in which parameters of three applications (Application #1, Application #2 and Application #3) are represented as vertical bars where the height of a bar indicates the value of the corresponding parameter. Applicants' specification at page 4, lines 30-32. In the example, the parameters include bandwidth, response time and capacity. Applicants' specification at page 4, line 33. The user may provide input via the display by positioning a cursor over a selected one of the vertical bars, depressing control key, such as a mouse button, and then lengthen or shorten the bar by moving the cursor (this technique may be referred to as "clicking and dragging"). Applicants' specification at page 5, lines 16-19. Based on this teaching, a person of ordinary skill in the art to which the invention pertains would certainly be able to implement the "receiving" step of claim 1 without having to resort to undue experimentation. Therefore, this step is enabled by the applicants' specification.

Claim 1 also recites steps of:

modifying the design in response to said desired levels including modifying the assignments of the system resources;

predicting levels of performance parameters for the modified design;...

As explained at page 5, lines 24-26 of the applicants' specification, in response to a user changing the displayed parameters, the design may be altered to accommodate the change. For example, a storage system design may only have a specified total amount of storage capacity. Applicants' specification at page 5, lines 26-27. Accordingly, if the user changes the capacity parameter for Application #1, this may affect the capacity available to Applications #2 and #3. Applicants' specification at page 5, lines 27-29.

To further illustrate this, the applicants' specification explains that if the user increases the capacity parameter for Application #1 and this increase results in a reduction of the capacity available to Applications #2 and #3 such that their capacity requirements may still be met using a modified design, the display may be updated to reflect new capacity parameters for Applications #2 and #3. Applicants' specification at page 5, line 33, to page 6, line 2. Alternatively, if this increase would not leave sufficient capacity for either Application #2 or #3, then an error message may be displayed or the requirements for the other applications may be modified in order to accommodate the user's desired changes. Applicants' specification at page 6, lines 3-13. One approach is to reduce the corresponding delivered performance parameter for all the other applications evenly (e.g., by the same percentage or amount). Applicants' specification at page 6, lines 14-16. For example, assume that the user desires to increase the capacity of Application #1, which requires freeing up three Gigabytes. Applicants' specification at page 6, lines 16-18. Assume also that Application #2 has a requirement of ten Gigabytes and that Application #3 has a requirement of twenty Gigabytes. Applicants' specification at page 6, lines 18-19. Under these circumstances, one option is to reduce the requirement of Application #2 by one Gigabyte (i.e. 10% of ten Gigabytes) and to reduce the requirement of Application #3 by two Gigabytes (i.e. 10% of twenty Gigabytes). Applicants' specification at page 6, lines 19-22. Another option is to reduce the capacity requirement for each of Applications #2 and #3 by the same amount (one and one-half Gigabytes). Applicants' specification at page 6, lines 19-24.

In the example above, the step of modifying the design is accomplished by adjusting the allocations of storage capacity to the applications so that the user's desired levels (which are received in the prior step) become part of the design. Thus, if the user desires to increase the capacity for Application #1, this new allocation becomes part of the design. The user may also make changes for Applications #2 and #3. And, in the example, the step of predicting performance levels for the modified design may be accomplished by comparing the adjusted allocations to the total available capacity to determine whether the performance levels, as updated by the user, can be met by the design. If so, the predicted performance levels are the same as the desired performance levels. If not, capacity allocations may be reduced so that the predicted performance levels are somewhat less than the desired levels.

Based on this teaching, a person of ordinary skill in the art to which the invention pertains would certainly be able to implement the modifying and predicting steps of claim 1 without having to resort to undue experimentation. As a simple example, the capacity allocation for each application can be represented by a different variable. Particularly, the capacity for application #1 can be represented by a variable x; the capacity for application #2 can be represented by a variable y; and the capacity for application #3 can be represented by a variable z. The values of the variables x, y and z may be displayed in a bar graph. The maximum capacity available can be represented by yet another variable m. When a user increases the value of one of the variables via the user interface (e.g., by manipulating the bar graph) a software routine can then sum the x, y and z variables to determine whether the sum exceeds the value m, which represents the maximum capacity available.

Of course, more complicated schemes could be implemented as well. As explained in the applicants' specification, a conventional computer aided design tool could be used to assign resources for the design. Applicants' specification at page 9, line 34 to page 10, line 7. A particular example of such a design tool is described in U.S. Patent Application Serial No. 09/924,735, which is incorporated into the application by reference. This application describes a tool for configuring a storage array and assigning data stores to various elements of the array. Applicants' specification at page 10, lines 5-7. Further, manual design techniques may be employed, such that the system is designed completely or partially "by hand." Applicants' specification at page 10, lines 8-9. Computer aided modeling techniques could also be used to determine whether a particular design provides the performance

parameter(s) specified by the user. Applicants' specification at page 10, lines 10-23. A particular example of such a modeling technique is described in U.S. Patent Application Serial No. 09/843,903, which is incorporated into the application by reference. This application describes a method and apparatus for morphological modeling of complex systems to predict performance. Applicants' specification at page 10, lines 20-21. Also, actual performance of a system constructed in accordance with the design could be measured to determine whether a particular design provides the performance parameter(s) specified by the user. Applicants' specification at page 10, lines 23-24.

In sum, the applicants' specification provides a detailed teaching, including an example, of how these steps may be performed, and gives examples of alternatives, including employing conventional design and modeling tools and conventional manual techniques.

Claim 1 also recites a step of:

displaying for the user an indication of the predicted levels of performance parameters for the modified design via the user interface

As explained for the example above, if the user's modification would not provide sufficient capacity for either Application #2 or #3, then an error message, such as "insufficient resources available" may be displayed to indicate that the predicted levels of performance parameters fall below the desired levels. Applicants' specification at page 6, lines 3-5. Further, the parameters for which the application requirements could not be met may change color on the display 100. Applicants' specification at page 6, lines 5-7. In addition, how much of the requirement that could not be met may be represented by using two colors: one showing the amount of a parameter available to an application and the other showing a difference between the amount of the parameter available and the minimum requirement for the application. Applicants' specification at page 6, lines 7-10. Based on this teaching, a person of ordinary skill in the art to which the invention pertains would certainly be able to implement the "displaying" step of claim 1 without having to resort to undue experimentation. Therefore, this step is enabled by the applicants' specification.

In view of the above, the applicants respectfully request that the rejection under 35 U.S.C. § 112, first paragraph, be removed.

Rejections under 35 U.S.C. § 102:

Claims 1-5, 10-16, 21-22 and 23-27 are rejected under 35 U.S.C. § 102 as being anticipated by Douglas J. Smith, "HDL Chip Design - A practical guide for designing, synthesizing and simulating ASICs and FPGAs Using VHDL or Verilog" (hereinafter, "Smith").

The applicants respectfully traverse the rejection. Smith explains that both application specific integrated circuits (ASICs) and Field Programmable Gate Arrays (FPGAs) are types of integrated circuits whose functions are defined by a designer. Smith at page 3. There are two categories of ASICs; gate arrays and standard cells. Smith at page 4. Gate arrays have a library of basic cells, such a logic gates, registers and macros, whereas, standard cells do not have components prefabricated on the chip. Smith at page 4. FPGAs is a completely manufactured device that is design independent and includes a number of programmable logic blocks connected to programmable switching matrices. Smith at page 4. Smith explains that a top-down design methodology takes a hardware description language (HDL) model of hardware, written at a high level of behavioral abstraction, down through intermediate levels, to a low (gate or transistor) level. Smith at pages 5-6. As hardware models are translated to progressively lower levels they become more complex and contain more structural detail. Smith at page 7.

Smith further explains that HDL is a software programming language used to model the intended operation of a piece of hardware. Smith at page 8. Two aspects to the description include behavior modeling and hardware structure modeling. Smith at page 8. Smith describes the history of two HDLs, VHDL and Verilog, and compares the two. Smith at pages 8-14. Smith then explains that simulation is used for ASIC and FPGA design to verify functional characteristics. Smith at page 14. Fault simulation is used to identify areas of a circuit not being functionally tested by functional test vectors, to check quality of test vectors and to perform board and in-circuit chip testing for both production and repair testing. Smith at page 15. Smith then describes the use of register transfer level (RTL) synthesis to translate an RTL model of hardware, written in a hardware description language into an optimized technology specific gate-level implementation. Smith at pages 17-19.

As explained above, claim 1 recites a method of assigning resources for a computer system design comprising: receiving desired levels of performance

parameters for a computer system design from a user via a user interface to a computer system, the design including assignments of system resources to applications; modifying the design in response to said desired levels including modifying the assignments of the system resources; predicting levels of performance parameters for the modified design; and displaying for the user an indication of the predicted levels of performance parameters for the modified design via the user interface.

Claim 1 is allowable over Smith at least because Smith does not suggest or disclose such steps. For example, Smith does not disclose receiving desired levels of performance parameters from a user via a user interface. The office action relies on Figures 1.3, 1.4 and 1.14 of Smith as disclosing this feature. However, Figure 1.3 merely shows a design model domain for different levels of abstraction in the design of a hardware circuit, while Figure 1.4 merely shows an ASIC design flow using simulation and RTL synthesis. Figure 1.14 of Smith shows an RTL synthesis internal translation and optimization process. Nowhere does Smith suggest or disclose receiving desired performance levels. Because Smith does not suggest or disclose receiving desired performance parameters from a user, Smith also can not disclose modifying an existing design based on received desired performance parameters. Smith also does not suggest or disclose that the design might include assignments of system resources to applications.

Further, Smith does not disclose predicting levels of performance parameters for such a modified design. While Smith does discuss models, they are used for verifying functional characteristics and for fault testing. The office action also relies on Figures 1.3, 1.4 and 1.14 of Smith as disclosing this feature. Nowhere does Smith suggest or disclose predicting performance parameters.

Further, Smith does not disclose displaying for the user an indication of the predicted levels of performance parameters for the modified design via the user interface. The office action, in relying again on Figures of Smith 1.3, 1.4 and 1.14 of Smith as disclosing this feature states that Figure 1.4 states "'Results compare' which means that the modified design results are compared to the desired results." Even if this is correct, this does not suggest or disclose displaying an indication of the predicted levels of performance parameters. Because Smith does not disclose predicting levels of performance parameters, Smith cannot suggest or disclose

displaying for a user an indication of such predicted levels of performance parameters.

For at least these reasons, claim 1 is allowable over Smith. Claims 2-5 are allowable at least because they are dependent from claim 1. Moreover, these dependent claims recite features not suggested or disclosed by Smith. For example, claim 2 recites that the computer system design comprises a design for a data storage system. In contrast Smith is directed to use of HDL tools for designing ASICs and FPGAs. The ASICs and FPGAs of Smith are not data storage systems. Smith also does not teach that HDL tools could be applied to the design of a data storage system, nor to the design of a data storage system that includes assignments of system resources to applications. Claims 4 and 5 recite utility functions representing utility as a function of one or more performance parameters. Smith does not suggest or disclose utility functions.

Claim 10 recites a method of assigning resources for a computer system design comprising: receiving desired levels of performance parameters for a computer system design from a user via a user interface to a computer system; developing the design including assignments of system resources to applications; predicting levels of performance parameters for the design; comparing the predicted levels of performance parameters to the desired levels of performance parameters; modifying the design including modifying the assignments of the system resources when the predicted levels are lower than the desired levels, said modifying being performed by the computer system; and displaying for the user results of the modifying via the user interface.

Thus, similarly to claim 1, claim 10 recites receiving desired levels of performance parameters for a computer system design from a user via a user interface and predicting levels of performance parameters for the design. Claim 10 also recites that the design includes assignments of system resources to applications. As explained above, Smith does not suggest or these features.

Claim 10 also recites comparing the predicted levels of performance parameters to the desired levels of performance parameters, modifying the assignments of the system resources when the predicted levels are lower than the desired levels and displaying for the user results of the modifying via the user interface. The office action again relies on Figures 1.3, 1.4 and 1.14 of Smith as disclosing these features. However, because Smith does not disclose predicting levels

of performance parameters, Smith cannot suggest or disclose comparing the predicted levels of performance parameters or modifying assignments of system resources based on results of such comparing or displaying for the user results of the modifying.

For at least these reasons, claim 10 is allowable over Smith. Claims 11-16 and 21-22 are allowable at least because they are dependent from claim 10.

Claim 23 recites an apparatus for assigning resources for a computer system design, comprising a computer system programmed to operate in a first program loop in which a user specifies desired levels of performance parameters of the design via a user interface and a second program loop in which: performance parameter levels are predicted for the design; the predicted performance parameters are compared to the desired levels of performance parameters; the design is modified, including modifying the assignments of system resources to applications, in response to the comparison and results of the modifying are displayed for the user via the user interface.

Thus, claim 23 requires a first program loop in which a user specifies desired levels of performance parameters of the design via a user interface. As explained above, Smith does not teach or suggest receiving performance parameters from a user. Thus, Smith does not teach or suggest this claim feature.

As explained above, Smith does not suggest or disclose predicting levels of performance parameters. Therefore, Smith cannot suggest or disclose comparing the predicted levels of performance parameters or modifying assignments of system resources to applications based on results of such comparing or displaying for the user results of the modifying, all of which are required by claim 23.

For at least these reasons, claim 23 is allowable over Smith. Claims 24-27 are allowable at least because they are dependent from claim 23.

Rejections under 35 U.S.C. § 103:

Claims 6-9, 17-20 and 28-31 are rejected under 35 U.S.C. § 103 as being unpatentable over Smith in view of U.S. Patent No. 6,449,761 to Greidinger et al. (hereinafter, "Greidinger").

The applicants respectfully traverse the rejection. It should be noted that claims 6-9, 17-20 and 28-31 are each dependent from an allowable base claim 1, 10 or 23. As explained above, claims 1, 10 and 23 are allowable because Smith does not suggest or disclose all of the limitations of these claims. Greidinger is directed toward circuit aided design for circuit layout and does not suggest or disclose all of

the limitations missing from Smith. For example, Greidinger does not suggest or disclose that the design includes assignments of system resources to applications, as in claims 1, 10 and 23.

Therefore, claims 1, 10 and 23 are allowable over Smith and Greidinger, taken singly or in combination. Claim 6-9, 17-20 and 28-31 are allowable over Smith and Greidinger at least because they each depend from an allowable base claim 1, 10 or 23. Moreover, these dependent claims recite features not suggested or disclosed by Smith or Greidinger. For example, claims 7-9, 18-20 and 29-31 require that desired levels of performance parameters be specified by the user manipulating heights of bar graphs shown on a display of the computer system. Neither Smith nor Greidinger suggest or disclose such a feature.

Conclusion:

In view of the above, the applicants submit that all of the pending claims are now allowable. Allowance at an early date would be greatly appreciated. Should any outstanding issues remain, the examiner is encouraged to contact the undersigned at (408) 293-9000 so that any such issues can be expeditiously resolved.

Respectfully Submitted,

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Derek J. Westberg (Reg. No. 40,872)